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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	Confirmation Number: 6219
Hiroshi TAKENO	Group Art Unit: 1722
Application No.: 09/926,202	Examiner: G. Nagesh Rao
Filed: September 24, 2001	Attorney Dkt. No.: 107242-00024

For: MANUFACTURING PROCESS FOR SILICON EPITAXIAL WAFER

RESPONSE UNDER 37 C.F.R. § 1.116

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 17, 2007

Sir:

The Office Action dated April 17, 2007, has been received and carefully noted. The following remarks are being submitted as a full and complete response thereto. Reconsideration of the rejections is respectfully requested in light of the following remarks. Claims 7-9, 14-17 and 22 are pending in this application.

The Office Action rejects claims 7-9, 14-17 and 22 under 35 U.S.C. § 102(b)/103(a) over Miyashita et al. (U.S. Patent No. 5,951,755); and claims 7-9, 14-17 and 22 under 35 U.S.C. § 103(a) over Wijaranakula (U.S. Patent No. 5,611,855) in view of Wolf et al. (Silicon Processing for the VLSI Era); Volume 1: Process Technology, Lattice Press, Sunset Beach, California, pages 26-30, 59-61, 124 and 133-136). The rejections are respectfully traversed.

In particular, the above-identified application claims a manufacturing process for a silicon epitaxial wafer that includes the steps of providing a silicon substrate, forming an epitaxial layer over the silicon substrate and forming new oxygen precipitation nuclei